REMARKS/ARGUMENTS

Present Status of Application

Claims 1-10 are pending.

It is Examiner's belief that claims 1-10 are rejected under 35 U.S.C. 103(a). Applicant respectfully traverses the rejections made by the Examiner for the reasons discussed below.

35 U.S.C. 103(a)

It is Examiner's belief that claims 1 and 3-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (U.S. Patent No. 6,606,088) in view of Kai et al. (Pub. No.: US 2002/0122041) and further in view of Nakano et al. (U.S. Patent No. 6,229,513). The Examiner admits that Yang differs from claim 1 in that he does not specifically teach the control signal that controls the scale module, and Kai teaches a micro-processing device (MPU 46) adapted to output a control signal that controls the scale module (timing pulse generation circuit 43).

Referring to claim 1 of the present invention, **the scale module is provided to receive the first digital video signal** and the micro-processing device is adapted to output a first control signal that controls the scale module to generate a gate/source-driving signal for the gate driver and source driver **based on the first digital video signal**. However, in Kai's patent, an video signal VB is converted from a signal processing circuit 20 to the data driver 30 (see paragraph [0044]) directly without processing through the scale module (timing pulse generation circuit 43). As

the output pixel clock CLKD are individually transferred to the data drier 30, wherein the video signal VB is never processed through the control circuit 40. Therfore, Kai fails to teach or disclose "**the scale module provided to receive the first digital video signal**" as claimed in claim 1. Further, in Kai's invention, the MPU 46 is provided with a table ROM, comparing the horizontal cycle time TH and vertical cycle time TF coming from the cycle time detecting circuit 45 with the data in the table ROM. It is provided only for determining the q and p values to generate the pixel clock CLKD (see paragraph [0064]) without any video signal involved. That is, Kai fails to teach or disclose "the micro-processing device adapted to output a first control signal that controls the scale module to generate a gate/source-driving signal for the gate driver and source driver **based on the first digital video signal**". Therefore, as the timing pulse generation circuit 43 and MPU 46 in Kai's patent cannot be equal to the scale module 22 and MPD 23 of the present invention, Applicant notes that the Examiner's rejection does not provide an element by element analysis of claim 1.

Though Nakano disclosed an LCD apparatus with shield cases LF1, LF2 and SHD, Applicant notes that Nakano fails to teach, nor would it have been obvious to use "the scale module provided to receive the first digital video signal" and "the micro-processing device adapted to output a first control signal that controls the scale module to generate a gate/source-driving signal for the gate driver and source driver based on the first digital video signal" as disclosed in claim 1 of the present invention.

As mentioned above, the Examiner does not appropriately indicate each corresponding element in claim

1 of the present application. That is, neither Yang, Kai nor Nakano disclose all the elements mentioned above in claim 1, and Applicant notes that there is no motivation and it has not been taught or suggested to combine these three cited references to use the scale module provided to receive the first digital video signal and the micro-processing device adapted to output a first control signal that controls the scale module to generate a gate/source-driving signal for the gate driver and source driver based on the first digital video signal as claimed in claim 1 of the present invention. It is therefore Applicant's belief that claim 1 is allowable over the cited references.

Insofar as claims 3-10 depend from claim 1, it is Applicant's belief that these claims are also allowable.

Dalgleish (U.S. Patent No. 6,373,476) discloses a video signal comprising an EDID signal, however, he fails to teach or suggest the scale module and the micro-processing device as claimed in claim 1 of the present invention. Insofar as claim 2 depends from claim 1, it is Applicant's belief that claim 2 is also allowable.